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(FILE 'USPAT' ENTERED AT 10:22:02 ON 19 NOV 96)

L1 0 S (GROUP? (5A) (PERIPHERAL# OR I O OR INPUT OUTPUT) (5A) (
SIM
L2 0 S (GROUP ORDER?)/TI,AB
L3 900 S (FAMILY (5A) DEVICE#)
L4 87 S L3 (P) (GROUP? OR SET#)
L5 6825 S (PLURALITY OR MULTIPLE) (5A) INTERFACE#
L6 1 S L4 AND L5
L7 3029 S L5/TI,AB,CLM
L8 701 S L5/TI,AB
L9 4793 S (PLURALITY OR MULTIPLE) (3A) INTERFACE#
L10 494 S L9/TI,AB
L11 0 S L4 AND L10
L12 4 S L3 AND L10
L13 1063 S (PLURALITY OR MULTIPLE) (2A) INTERFACES
L14 87 S L13/TI,AB
L15 1 S L3 AND L14
L16 5 S L13 (5A) APPLICATION
L17 18 S L13 (5A) (SEPARATE OR INDIVIDUAL OR DISTINCT)
L18 0 S L3 AND L17
L19 9315 S (GROUP# (5A) DEVICE#)
L20 0 S L17 AND L19
L21 49 S L13 AND L19
L22 6 S L13 (P) L19
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US PAT NO: 4,727,537 [IMAGE AVAILABLE] L22: 6 of 6
TITLE: Flow control arrangement for the transmission of data
packets to a communication network

CLAIMS:

CLMS(1)

What is claimed is:

1. A packet data bus interconnecting a plurality of data transmitting and receiving devices via a ****plurality**** of ****interfaces**** where each interface control bus access for the transmission of data packets over said bus from a ****group**** of associated ****devices****, a flow control arrangement for controlling the flow of data packets through said interface comprising:

an interface processor for processing data transmissions;
an interface buffer for storing a plurality of data packets received from said ****group**** of ****devices**** associated with said interface;
means including said interface processor for detecting when said interface buffer contains insufficient space to store a. . . said interface processor and responsive to a detection of insufficient space for inhibiting the transmission of data packets by said ****group**** of ****devices**** associated with said interface.

CLAIMS:

CLMS(8)

8. A packet data bus interconnecting a plurality of data transmitting and receiving devices via a ****plurality**** of ****interfaces**** where each interface controls bus access for the transmission of data packets over said packet data bus from a ****group**** of associated ****devices**** to said network, a method for controlling the flow of data packets through said interface to said packet data bus, . . .

said interface buffer contains insufficient space to accommodate a specified maximum length data packet transmitted from any one of said ****group**** of ****devices**** associated with said interface;
generating a jam signal when said interface buffer contains insufficient space to store a next transmitted maximum length data packet; and
applying said jam signal to said ****group**** of ****devices**** to inhibit any further transmission of data packets from said ****group**** of ****devices****.

CLAIMS:

CLMS(9)

9. A packet data bus interconnecting a plurality of data transmitting and receiving devices via a ****plurality**** ****interfaces**** where each interface controls bus access for the transmission of data packets over said packet data bus from a ****group**** of associated ****devices****, a method for controlling the flow of data packets through said interface to said packet data bus, wherein said method. . .

US PAT NO: 5,553,245 [IMAGE AVAILABLE] L12: 1 of 4
TITLE: Automatic configuration of **multiple** peripheral
interface subsystems in a computer system
TITLE: Automatic configuration of **multiple** peripheral
interface subsystems in a computer system

ABSTRACT:

An apparatus for automatic configuration of **multiple** peripheral
interface subsystems in a computer system, the computer system
including a system expansion bus for adopting a **plurality** of
functional peripheral **interface** subsystems, the apparatus comprises a
software identification code buffer for buffering a software-generated
identification code sent via the system expansion. . .

CLAIMS:

CLMS (1)

What . . .
first prespecified offset address, which when accessed across the
peripheral bus returns a device type identifier for the particular
peripheral **device**;
a **family** store, accessible across the peripheral bus and having a
second prespecified offset address, which when accessed across the
peripheral bus. . . in the particular cycle in the autoconfiguration
process, by storing a family value corresponding to the particular
cycle in the **device** **family** store, or if the lock control signal
is asserted when the autoconfigure instruction is received by
maintaining the family value corresponding to a previous cycle in the
device **family** store; and
the control processor responding to a lock enable instruction indicating
successful access to the signature store and the family. . .

CLAIMS:

CLMS (5)

5. . . .
first prespecified offset address, which when accessed across the
peripheral bus returns a device type identifier for the particular
peripheral **device**;
a **family** store, accessible across the peripheral bus and having a
second prespecified offset address, which when accessed across the
peripheral bus. . . in the particular cycle in the
autoconfiguration process, by storing a family value corresponding to
the particular cycle in the **device** **family** store, or if the
lock control signal is asserted when the autoconfigure instruction is
received by maintaining the family value corresponding to a previous
cycle in the **device** **family** store; and
the control processor responding to a lock enable instruction
indicating successful access to the signature store and the family. .

CLAIMS:

CLMS (6)

6.
state issues a predictor in a sequence of predictors, then
in a second state attempts to access the signature store and **family**
store of a peripheral **device** on the peripheral bus using a base
address corresponding to the cycle of the autoconfiguration process,
and
if the access. . . . access to the signature store is not successful,
then issues the autoconfigure instruction before changing the
predictor to separate the **family** values in the peripheral
devices which do not match from the **family** value in a
peripheral **device** which does match the predictor, and then changes
the predictor and returns to the second state in an iterative fashion.

CLAIMS:

CLMS(10)

10.
the enabling step using a different network identifier predictor for a
next network interface device in the multiple network interface
devices,
if the **family** value is read but not the signature value, then
causing the family value of the particular network interface
device to be different than the **family** value in other ones of
the multiple network interface devices, and returning to the
attempting step,
if neither the family value. . . .

CLAIMS:

CLMS(11)

11. device to be different, comprises issuing an autoconfigure
instruction without changing the network identifier predictor, causing
the particular network interface **device** to maintain the same
family value, while family values stored in other network interface
devices change in response to the autoconfigure instruction.

US PAT NO: 5,313,618 [IMAGE AVAILABLE] L12: 2 of 4
TITLE: Shared bus in-circuit emulator system and method

ABSTRACT:

An emulation processor having I/O ports and a multiplexed
address/data bus port, an emulation memory having address inputs, a data
bus **interface** and a **plurality** of two-to-one multiplexers. The
in-circuit emulator is configured such that the control processor and the
emulation processor each have at. . . .

DETDESC:

DETD(21)

PORT4 PORT0 and PORT2 (shown respectively as "P0" and "P2")
which are active in fetching external instructions and data (in 8051
family **devices**). PORT0 of emulation processor 204 is coupled
directly to shared data bus 210. The data inputs of address latch 212. . .

US PAT NO: 5,285,381 [IMAGE AVAILABLE] L12: 3 of 4
TITLE: Multiple control-point control system and method of use

ABSTRACT:

A fault tolerant control of a multiple control-point apparatus is disclosed. The system comprises: a host subsystem acting as a user ****interface****; a ****plurality**** of control-point actuators; a master controller subsystem which receives initialization data from the host terminal and which generates behavior commands;. . . .

DETDESC:

DETD(28)

A typical member in the transputer product ****family**** is a monolithic ****device**** containing an integer processor, fast memory and multiple serial communication links, which provide point-to-point connection between transputers. Link communications run. . . .

US PAT NO: 4,982,325 [IMAGE AVAILABLE] L12: 4 of 4
TITLE: Applications processor module for interfacing to a database system

ABSTRACT:

The personnel. An Applications Processor Microcomputer (APM) module includes a General Data Transport (GDT) to provide a powerful microprocessing environment and ****multiple**** data communication ****interfaces****, and an Applications Interface Module (AIM) to provide the appropriate signal interface with the database system, the GDT, and the. . . .

DETDESC:

DETD(5)

Processor (DTACK) signal when it presents or receives data, and normally all 68000 compatible peripherals generate this signal internally. For non-68000 ****family**** ****devices****, such as an EPROM and EEROM located in memory module 22 and GPIB controllers in ICM 24, a DTACK generation. . . .

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